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Inside the New Record-Breaking 11-Qubit Processor From Silicon Quantum Computing

Computing * Energy * Physics

The Silicon Imperative and the Fault-Tolerant Threshold

For decades, the engineering of practical quantum computers has been constrained by decoherence -- the rapid collapse of fragile quantum superpositions due to thermal and electromagnetic noise. Across the global hardware landscape, competing physical modalities have faced steep trade-offs between gate speed, coherence lifetime, and manufacturability. Superconducting transmon processors championed by Google and IBM offer nanosecond gate speeds and hundreds of physical qubits, yet suffer from microsecond coherence windows and large ~100 m device footprints. Conversely, trapped-ion architectures developed by IonQ and Quantinuum achieve exceptional gate fidelities and second-scale coherence, but rely on complex optical switching and vacuum apparatus that complicate high-density scaling.[1]

Against these modalities, solid-state spin qubits in silicon have long promised unmatched atomic miniaturization and compatibility with semiconductor fabrication, provided researchers could overcome the magnetic noise of natural silicon lattices and the geometric bottleneck of wiring nanometer-spaced qubits.[1][2] In a landmark study published in Nature in December 2025, researchers at Silicon Quantum Computing (SQC) -- spun out of the University of New South Wales (UNSW) in Sydney under Professor Michelle Simmons -- resolved both obstacles simultaneously.[1][2][7] Operating an atomically fabricated 11-qubit processor built on their proprietary "14|15 platform" (silicon-28 host, atomic number 14; phosphorus-31 dopant qubits, atomic number 15), the SQC team demonstrated single-qubit gate fidelities up to 99.99% and two-qubit entangling gate fidelities up to 99.90% across linked multi-qubit registers.[2] By operating well above the ~99% fidelity threshold required for Surface Code quantum error correction, this device establishes atomic silicon as a premier contender for fault-tolerant commercial quantum computing.[2]

Quantum Physics of the 14|15 Platform: Isotopic Silicon-28 and Phosphorus-31 Spins

The coherence performance of the SQC processor originates in its foundational materials engineering. Natural minerally sourced silicon consists of ~92.2% 28Si (which has zero nuclear spin), ~3.1% 30Si (zero nuclear spin), and ~4.7% 29Si, whose spin-1/2 atomic nucleus generates a fluctuating magnetic bath that rapidly dephases embedded electron and nuclear spins via flip-flop dipole interactions.[2] To eliminate this magnetic decoherence channel, SQC fabricates its processor on isotopically enriched 28Si substrates in which the concentration of spin-bearing 29Si is depleted below 200 parts per million (ppm).[2] This magnetically silent crystalline lattice acts as a solid-state "semiconductor vacuum," extending spin coherence lifetimes by several orders of magnitude.

Within this purified 28Si host, individual phosphorus-31 (31P) donor atoms substitute for silicon lattice sites. Because phosphorus possesses five valence electrons compared to silicon's four, four electrons form covalent sp3 bonds with adjacent silicon atoms while the fifth unpaired donor electron remains loosely bound in a hydrogenic Bohr orbit of ~2-3 nm radius.[2] The 11-qubit processor encodes primary quantum data within nine 31P spin-1/2 nuclei (n1 through n9), paired with two shared donor electrons (e1 and e2) that act as ancillary control and coupling buses.[2]

Because the 31P nuclear spin is deeply shielded inside the donor electron cloud and immune to direct electric-field fluctuations, it achieves coherence times (T2) of up to 660 milliseconds inside the 11-qubit device -- yielding a ratio of coherence time to microsecond gate duration approaching 106 consecutive operations.[2] To read, write, and entangle these isolated nuclear spins, the architecture exploits the contact hyperfine interaction (A I * S) coupling each 31P nucleus (I) to its bound donor electron (S). Because the electron carries a magnetic moment roughly 2,000 times larger than the nucleus and a delocalized wavefunction spanning several nanometers, applying local electrostatic gate voltages deforms the electron cloud via the Stark effect.[3][4] This tunes the electron-nucleus wavefunction overlap in real time, allowing operators to decouple nuclear spins during idle memory storage and selectively recouple them to the electron handle during microwave and radio-frequency (RF) gate execution.[2][3]

Sub-Nanometer Fabrication via STM Hydrogen Lithography

Unlike conventional complementary metal-oxide-semiconductor (CMOS) ion implantation -- which shoots dopant ions into silicon wafers stochastically, producing random spatial variations that scramble inter-qubit coupling strengths -- SQC constructs its processor deterministically using Scanning Tunneling Microscope (STM) hydrogen lithography.[1][6] The three-stage atomic manufacturing pipeline proceeds inside an ultra-high vacuum (UHV) chamber:

* Monolayer Hydrogen Passivation and STM Desorption: An atomically flat 28Si wafer is passivated with a uniform monoatomic layer of hydrogen that serves as a chemical resist. Using an atomically sharp metallic STM tip biased with a controlled tunneling voltage, researchers selectively desorb individual hydrogen atoms with 0.13 nm spatial precision, exposing reactive silicon dangling bonds at the exact lattice coordinates designated for qubit registers and planar phosphorus control gates.[1][6]

* Phosphine Dosing and Thermal Incorporation: The patterned surface is dosed with phosphine (PH3) gas, which adsorbs exclusively onto the depassivated silicon sites while bouncing off the surrounding hydrogen resist. A rapid thermal anneal dissociates the PH3 molecules and incorporates the 31P atoms substitutionally into the silicon crystal lattice.[5]

* Locking Epitaxial Overgrowth: After removing the remaining hydrogen resist, the donor arrays are encapsulated beneath dozens of nanometers of crystalline 28Si using low-temperature Molecular Beam Epitaxy (MBE). SQC's specialized epitaxial locking recipe prevents vertical or lateral dopant diffusion during crystal growth, locking the 3D atomic coordinates of the processor.[5][7]

Modular Register Architecture and the Exchange-Coupled Quantum Link

A central engineering breakthrough of the 11-qubit processor is its resolution of the "wiring fan-out problem." Because donor spin qubits sit only nanometers apart, routing an independent metallic control electrode to every individual atom in a million-qubit array is geometrically impossible. SQC overcomes this bottleneck by grouping phosphorus nuclei into multi-atom registers that share a single bound ancilla electron and a common set of electrostatic control gates.[2]

Specifically, the 11-qubit processor comprises two separated atomic registers: a 4P register containing four 31P nuclear spins (n1-n4) coupled to one shared electron (e1), and a 5P register containing five 31P nuclear spins (n5-n9) coupled to a second shared electron (e2), yielding nine nuclear data qubits and two electron ancilla qubits.[2] Despite sharing common control lines, every nucleus within a cluster experiences a distinct local hyperfine environment and Stark shift, splitting the nuclear magnetic resonance (NMR) spectrum into well-resolved addressing frequencies spanning 24.221 MHz, 24.450 MHz, and 24.534 MHz up to 123.026 MHz.[2] By applying frequency-division multiplexed RF pulses down the shared gate, the controller selectively rotates any target nuclear qubit without disturbing its neighbors.

To scale beyond a single cluster, the two registers are spaced ~15-20 nm apart and bridged by a voltage-controlled electron exchange interaction (J).[2] When the electrostatic barrier between the 4P and 5P registers is lowered, the wavefunctions of electrons e1 and e2 overlap, establishing a tunable weak-exchange coupling of J ~ 1.55 MHz.[2] Because direct exchange coupling is vulnerable to charge noise, the SQC team engineered a dynamical-decoupling "Sandwich" pulse protocol (X--Exchange--X) to execute inter-register Controlled-Z (CZ) gates between any nucleus in the 4P cluster and any nucleus in the 5P cluster.[2] By swapping nuclear states onto the local electrons and inserting -flip (X) pulses midway through the exchange time evolution, low-frequency phase errors cancel via spin echo.[2] Crucially, the researchers also discovered that activating the exchange link shifts all 96 conditional electron resonance frequencies collectively by a uniform offset; thus, measuring a single reference transition calibrates the entire multi-register spectrum, reducing calibration complexity from exponential to linear scaling.[2]

Experimental Fidelity Benchmarks and Modality Comparison

Evaluated via Randomized Benchmarking (RB) and quantum state tomography at ~15 millikelvin dilution refrigerator temperatures, the 11-qubit processor set new accuracy benchmarks for solid-state quantum hardware.[1][2] Single-qubit operations reached 99.99% fidelity (an error probability of 10-4), intra-register nuclear-nuclear CZ gates achieved up to 99.90% fidelity, and inter-register electron-mediated entangling operations reached 99.64% to 99.90% fidelity.[1][2] To validate system-wide multi-qubit quantum entanglement across the exchange link, the team deterministically generated entangled Bell states across registers with 99.5% fidelity and synthesized an 8-qubit Greenberger-Horne-Zeilinger (GHZ) Schr dinger-cat state spanning both registers.[2]

| Hardware Metric | | SQC Atomic Silicon (14|15 Platform) | | Superconducting Transmons (e.g., Google Willow) | | Trapped Atomic Ions (e.g., IonQ / Quantinuum) |

| Physical Qubit Carrier | | 31P Nuclear & Electron Spins in 28Si[2] | | Macroscopic Josephson Junction Loops | | Laser-Cooled Atomic Ions (e.g., 171Yb+) |

| Single-Qubit Footprint | | ~3 nm (Atomic register scale)[2] | | ~100 m (Millimeter chip pitch) | | Atomic (Micrometer trap electrode spacing) |

| Coherence Time (T2) | | Up to 660 ms (Seconds in isolated 28Si)[2] | | ~50-100 s | | >1-10 s |

| 1-Qubit Gate Fidelity | | 99.99% (Randomized Benchmarking)[1] | | 99.8% - 99.9% | | 99.99% - 99.999% |

| 2-Qubit Gate Fidelity | | 99.90% (Intra/Inter-register CZ)[2] | | 99.5% - 99.8% | | 99.8% - 99.9% |

| Characteristic Gate Speed | | Fast (s nuclear / ns electron) | | Very Fast (10-50 ns) | | Slow (100 s - ms) |

| Scalability & Fab Path | | High (Monolithic 2D register tiling)[7] | | Medium (Cryogenic I/O & footprint limits) | | Low-Medium (Complex 2D optical shuttling) |

Because these physical error rates (~0.01% to 0.1%) sit roughly an order of magnitude below the ~1% fault-tolerance threshold of the topological Surface Code, SQC can tile 2D arrays of 4P/5P registers (~17 linked registers, or ~85 physical qubits, per distance-3 logical qubit) without suffering exponential error accumulation.[2] This architectural roadmap underpins SQC's schedule to deploy a 100-qubit processor by 2030 and a commercial fault-tolerant quantum computer by 2033, supported by early enterprise partnerships with Telstra and the Australian Department of Defence -- alongside SQC's October 2025 launch and 2026 commercial expansion of its Watermelon quantum reservoir computing system for machine-learning feature generation.[1][7][8][9]

Conclusion: From Atomic Physics to Fault-Tolerant Scale

The demonstration of 99.99% single-qubit and 99.90% two-qubit gate fidelities across linked multi-nuclear registers in SQC's 11-qubit processor marks a decisive transition for silicon quantum computing from fundamental atomic physics to scalable systems engineering.[1][2] By combining magnetically silent 28Si, sub-nanometer STM hydrogen lithography, frequency-multiplexed shared register control, and collectively calibrated electron exchange links, the 14|15 platform resolves the wiring, crosstalk, and decoherence barriers that long constrained solid-state spin qubits -- charting a sovereign, high-density manufacturing pathway toward utility-scale fault-tolerant quantum computation.[2][8]

Updates... (Nov 23, 2026): Corrected author initials in Reference 5 from Zhang, X., Chang, X., Dan, J. to Zhang, C., Chang, S., Dan, Y. per CrossRef metadata (doi:10.1080/23746149.2020.1871407), clarified that SQC launched its Watermelon quantum reservoir computing system in October 2025 with 2026 commercial expansion, and added the October 16, 2026 SQC Watermelon announcement as Reference 9.

References

* [1] Quantum Zeitgeist (Dec 18, 2025). SQC's Silicon Processor Achieves 99.99% Fidelity With Scaling. --

https://quantumzeitgeist.com/sqc-silicon-quantum-scaling-fidelity/

* [2] Edlbauer, H., Wang, J., Huq, A. M. S., et al. (Dec 17, 2025). An 11-qubit atom processor in silicon. Nature, 648(8094), 569-575. -- https://doi.org/10.1038/s41586-025-09827-w

* [3] Savytskyy, R., Botzem, T., Fernandez de Fuentes, I., et al. (Feb 10, 2023). An electrically driven single-atom "flip-flop" qubit. Science Advances, 9(6), eadd9408. -- https://doi.org/10.1126/sciadv.add9408

* [4] Friesen, M. (May 9, 2005). Theory of the Stark Effect for P Donors in Si. Physical Review Letters, 94(18), 186403. -- https://doi.org/10.1103/PhysRevLett.94.186403

* [5] Zhang, C., Chang, S., Dan, Y., et al. (Jan 1, 2021). Advances in ultrashallow doping of silicon. Advances in Physics: X, 6(1), 1871407. -- https://doi.org/10.1080/23746149.2020.1871407

* [6] Fuechsle, M., Miwa, J. A., Mahapatra, S., et al. (Feb 19, 2012). A single-atom transistor. Nature Nanotechnology, 7(4), 242-246. -- https://doi.org/10.1038/nnano.2012.21

* [7] Bluefors (Sep 29, 2025). Silicon Quantum Computing - Precision at the Atomic Scale. -- https://bluefors.com/stories/silicon-quantum-computing-precision-at-the-atomic-scale/

* [8] Quantum Australia (Dec 16, 2025). UNSW leads quantum technology revolution for national benefit. -- https://www.quantum-australia.com/news/unsw-leads-quantum-technology

* [9] Silicon Quantum Computing (Oct 16, 2026). SQC's Watermelon Chip Named to TIME Best Inventions 2026. -- https://sqc.com/news/sqc-time-best-inventions-2026